WHAT IS CLAIMED IS:

1. A non-volatile memory device, comprising:

a flash memory having a plurality of banks and a bank selection register which can take on states at least equal in number to the number of said banks and which outputs a signal for pointing to one of said banks corresponding to one of said states; and

a controller having a plurality of data buffers, each of which corresponds to one of said banks, respectively,

wherein each of said banks includes a plurality of word lines, a plurality of bit lines arranged to intersect said word lines, a plurality of memory cells, each of which is located at intersections of one of the word lines and one of the bit lines, and a data register which temporarily holds the data to be written to said memory cells, and

wherein said controller transmits the data in said data buffer to said data register of said one bank, while said flash memory writes the data held in said data register of another one of said banks to said memory cells thereof.

2. A non-volatile memory device according to claim 1, wherein said bank selection register can take on states greater in number than the number of said banks.

3. A non-volatile memory device according to claim 1, wherein said banks operate independently of one another.

4. A non-volatile memory device according to claim 2, wherein said banks operate independently of one another.

5. A non-volatile memory device according to claim 1, wherein said plurality of banks includes at least a first bank and a second bank, and wherein said bank selection register has at least a first state to produce a signal indicating that the first bank is selected and at least a second state to produce a signal indicating that the second bank is selected.

6. A non-volatile memory device according to claim 5, wherein said plurality of banks includes additional banks, other than said first and second banks, and wherein the number of states of the bank selecting register is greater in number than the number of said plurality of banks including the first and second banks and the additional banks.

7. A non-volatile memory device according to claim 1, wherein said controller receives read, write, erase and status polling commands and an address signal from outside said non-volatile memory device for the bank pointed to by the bank selection register.

8. A non-volatile memory device according to claim 7, wherein said controller includes means for converting said read, write, erase and status polling commands received from outside said non-volatile memory device into internal

control signals, and means for sending the internal control signals to the banks selected by said bank selection register.

9. A non-volatile memory device according to claim 1, wherein said bank selection register includes means for holding information in an unchanged condition regarding the state to point to a selected bank, based on information received from outside said non-volatile memory device, until other information is received from outside said bank selection register to change the state of said bank selection register.

10. A non-volatile memory device according to claim 9, wherein said banks operate independently of one another based upon the information received from said bank selection register from outside said non-volatile memory device.